TE0745 Test Board

Revision v.13

Exported on 2022-12-08

Online version of this document:

https://wiki.trenz-electronic.de/display/PD/TE0745+Test+Board

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4 Overview

Zynq Design PS with Linux and simple frequency counter to measure MGT Reference CLK with Vivado HW-Manager. Refer to http://trenz.org/te0745-info for the current online version of this manual and other available documentation.

4.1 Key Features

- Vitis/Vivado 2019.2
- PetaLinux
- SD
- ETH (MAC from EEPROM)
- USB
- I2C
- RTC
- FMeter
- Modified FSBL for SI5338 programming
- Special FSBL for QSPI programming

4.2 Revision History

Date	Vivado	Project Built	Authors	Description
2020-03-30	2019.2	TE0745-test_board-vivado_2019.2-build_8_20200330083452.zip TE0745-test_board_noprebuilt-vivado_2019.2-build_8_20200330083503.zip	John Hartfiel	• 2019.2 update • FSBL rework, SI5338 Project with Clock Builder pro • device tree update • Vitis support • new assembly variants
2018-09-2019	2018.2	TE0745-test_board_noprebuilt-vivado_2018.2-build_04_20190918103545.zip TE0745-test_board-vivado_2018.2-build_04_20190918103531.zip	John Hartfiel	• BUGFIX in TE0745-02-45-3EA board parts
2018-11-26	2018.2	TE0745-test_board-vivado_2018.2-build_03_20181126115131.zip TE0745-test_board_noprebuilt-vivado_2018.2-build_03_20181126115320.zip	John Hartfiel	• Rework Board Part Files • New assembly versions • Rework BD Design • add init.sh scripts

Date	Vivado	Project Built	Authors	Description
2017-10-23	2017.2	TE0745-test_board_noprebuilt-vivado_2017.2-build_05_20171023171903.zip TE0745-test_board-vivado_2017.2-build_05_20171023171855.zip	John Hartfiel	• initial release

Table 1: Design Revision History

4.3 Release Notes and Know Issues

Issues	Description	Workaround	To be fixed version
No known issues	---	---	---

Table 2: Known Issues

4.4 Requirements

4.4.1 Software

Software	Version	Note
Vitis	2019.2	needed, Vivado is included into Vitis installation
PetaLinux	2019.2	needed
SI ClockBuilder Pro	---	optional

Table 3: Software

4.4.2 Hardware

Basic description of TE Board Part Files is available on TE Board Part Files.[1]

Complete List is available on <design name>/board_files/*_board_files.csv

Design supports following modules:

1 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0745-02-30-1I	30_1i_1gb	REV02| REV01	1GB	32MB	NA	NA	smaller FPGA has less MGTs
TE0745-02-30-2IA	30_2i_1gb	REV02| REV01	1GB	32MB	NA	NA	smaller FPGA has less MGTs
TE0745-02-35-1C	35_1c_1gb	REV02| REV01	1GB	32MB	NA	NA	
TE0745-02-45-2I	45_2i_1gb	REV02| REV01	1GB	32MB	NA	NA	
TE0745-02-45-2IA	45_2i_1gb	REV02| REV01	1GB	32MB	NA	NA	
TE0745-02-45-1C	45_1c_1gb	REV02| REV01	1GB	32MB	NA	NA	
TE0745-02-45-1CA	45_1c_1gb	REV02| REV01	1GB	32MB	NA	NA	
TE0745-02-45-3EA	45_3e_1gb	REV02| REV01	1GB	32MB	NA	NA	
TE0745-02-93E11-A	45_3e_1gb	REV02	1GB	32MB	NA	NA	
TE0745-02-92I11-F	45_2i_ff_1gb	REV02	1GB	32MB	NA	NA	
TE0745-02-92I11-A	45_2i_1gb	REV02	1GB	32MB	NA	NA	
TE0745-02-91C11-A	45_1c_1gb	REV02	1GB	32MB	NA	NA	

Module Model	Board Part Short Name	PCB Revision Support	DDR	QSPI Flash	EMMC	Others	Notes
TE0745-02-81C11-A	35_1c_1gb	REV02	1GB	32MB	NA	NA	
TE0745-02-72I11-A	30_2i_1gb	REV02	1GB	32MB	NA	NA	smaller FPGA has less MGTs
TE0745-02-71I11-A	30_1i_1gb	REV02	1GB	32MB	NA	NA	smaller FPGA has less MGTs
TE0745-02-71I11-AK	30_1i_1gb	REV02	1GB	32MB	NA	NA	smaller FPGA has less MGTs

Table 4: Hardware Modules
Design supports following carriers:

Carrier Model	Notes
TEB0745	

Table 5: Hardware Carrier
Additional HW Requirements:

Additional Hardware	Notes
USB Cable for JTAG/UART	Check Carrier Board and Programmer for correct typ
XMOD Programmer	Carrier Board dependent, only if carrier has no own FTDI

Table 6: Additional Hardware

4.5 Content

For general structure and of the reference design, see Project Delivery - Xilinx devices[2]

4.5.1 Design Sources

2 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices

Type	Location	Notes
Vivado	<design name>/block_design <design name>/constraints <design name>/ip_lib	Vivado Project will be generated by TE Scripts
SDK/HSI	<design name>/sw_lib	Additional Software Template for Vitis and apps_list.csv with settings automatically for Vitis app generation
PetaLinux	<design name>/os/petalinux	PetaLinux template with current configuration

Table 7: Design sources

4.5.2 Additional Sources

Type	Location	Notes
SI5338	<design name>/misc/Si5338	Si5338 Project with current PLL Configuration
init.sh	<design name>/misc/sd	Additional Initialization Script for Linux

Table 8: Additional design sources

4.5.3 Prebuilt

File	File-Extension	Description
BIF-File	*.bif	File with description to generate Bin-File
BIN-File	*.bin	Flash Configuration File with Boot-Image (Zynq-FPGAs)
BIT-File	*.bit	FPGA (PL Part) Configuration File
DebugProbes-File	*.ltx	Definition File for Vivado/Vivado Labtools Debugging Interface

File	File-Extension	Description
Diverse Reports	---	Report files in different formats
Hardware-Platform-Specification-Files	*.xsa	Exported Vivado Hardware Specification for Vitis and PetaLinux
LabTools Project-File	*.lpr	Vivado Labtools Project File
OS-Image	*.ub	Image with Linux Kernel (On Petalinux optional with Devicetree and RAM-Disk)
Software-Application-File	*.elf	Software Application for Zynq or MicroBlaze Processor Systems

Table 9: Prebuilt files (only on ZIP with prebult content)

4.5.4 Download

Reference Design is only usable with the specified Vivado/SDK/PetaLinux/SDx version. Do never use different Versions of Xilinx Software for the same Project.

Reference Design is available on:

- TE0745 "test Board Reference Design[3]

3 https://shop.trenz-electronic.de/Download/?path=Trenz_Electronic/Modules_and_Module_Carriers/5.2x7.6/TE0745/Reference_Design/2019.2/test_board

5 Design Flow

> ⚠ Reference Design is available with and without prebuilt files. It's recommended to use TE prebuilt files for first lunch.

Trenz Electronic provides a tcl based built environment based on Xilinx Design Flow.

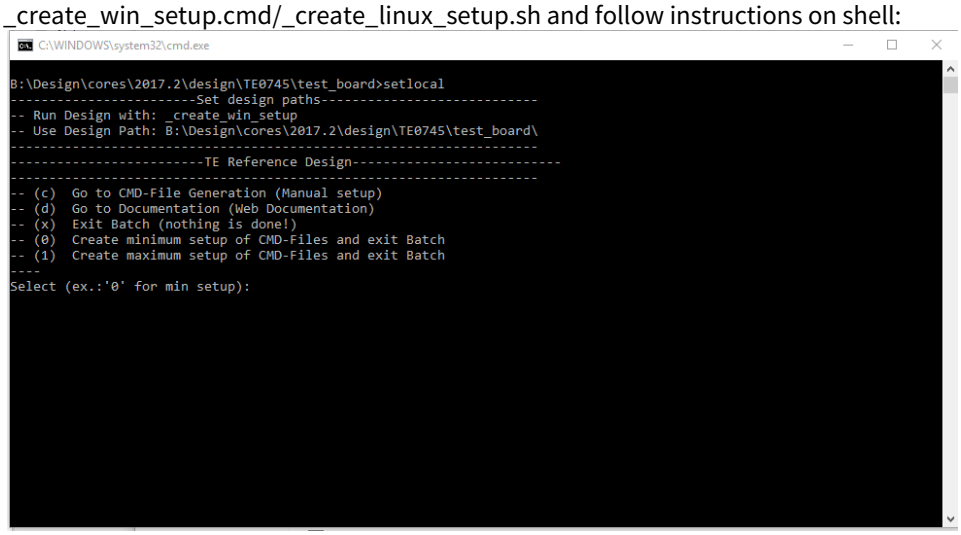
See also:

- Xilinx Development Tools[4]
- Vivado Projects - TE Reference Design[5]
- Project Delivery.[6]

The Trenz Electronic FPGA Reference Designs are TCL-script based project. Command files for execution will be generated with "_create_win_setup.cmd" on Windows OS and "_create_linux_setup.sh" on Linux OS.

TE Scripts are only needed to generate the vivado project, all other additional steps are optional and can also executed by Xilinx Vivado/SDK GUI. For currently Scripts limitations on Win and Linux OS see: Project Delivery Currently limitations of functionality[7]

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell:



2. Press 0 and enter to start "Module Selection Guide"
3. (optional Win OS) Generate Virtual Drive or use short directory for the reference design (for example x: \<design name>)
4. Create Project (follow instruction of the product selection guide), settings file will be configured automatically during this process)
   a. (optional for manual changes) Select correct device and Xilinx install path on "design_basic_settings.cmd" and create Vivado project with "vivado_create_project_guimode.cmd"
   Note: Select correct one, see TE Board Part Files[8]
5. Create XSA and export to prebuilt folder
   a. Run on Vivado TCL: TE::hw_build_design -export_prebuilt
   Note: Script generate design and export files into \prebuilt\hardware\<short dir>. Use GUI is the same, except file export to prebuilt folder
6. Create Linux (uboot.elf and image.ub) with exported XSA

4 https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftware-BasicUserGuides
5 https://wiki.trenz-electronic.de/display/PD/Vivado+Projects+-+TE+Reference+Design
6 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices
7 https://wiki.trenz-electronic.de/display/PD/Project+Delivery+-+Xilinx+devices#ProjectDeliveryXilinxdevices-Currentlylimitationsoffunctionality
8 https://wiki.trenz-electronic.de/display/PD/TE+Board+Part+Files

   a. XSA is exported to "prebuilt\hardware\<short name>"
      Note: HW Export from Vivado GUI create another path as default workspace.
      Create Linux images on VM, see PetaLinux KICKstart[9]
      i. Use TE Template from /os/petalinux
7. Add Linux files (uboot.elf and image.ub) to prebuilt folder
   a. "prebuilt\os\petalinux\<ddr size>" or "prebuilt\os\petalinux\<short name>"
8. Generate Programming Files with Vitis
   a. Run on Vivado TCL: TE::sw_run_vitis -all
      Note: Scripts generate applications and bootable files, which are defined in "sw_lib\apps_list.csv"
   b. (alternative) Start SDK with Vivado GUI or start with TE Scripts on Vivado TCL: TE::sw_run_vitis
      Note: TCL scripts generate also platform project, this must be done manuelly in case GUI is used. See Vitis[10]

9 https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart
10 https://wiki.trenz-electronic.de/display/PD/Vitis

6 Launch

6.1 Programming

⚠ Check Module and Carrier TRMs for proper HW configuration before you try any design.

Xilinx documentation for programming and debugging: Vivado/SDK/SDSoC-Xilinx Software Programming and Debugging[11]

6.1.1 Get prebuilt boot binaries

1. _create_win_setup.cmd/_create_linux_setup.sh and follow instructions on shell
2. Press 0 and enter to start "Module Selection Guide"
   a. Select assembly version
   b. Validate selection
   c. Select Create and open delivery binary folder
   Note: Folder (<project foler>/_binaries_<Artikel Name>) with subfolder (boot_<app name>) for different applications will be generated

6.1.2 QSPI

Optional for Boot.bin on QSPI Flash and image.ub on SD.

1. Connect JTAG and power on carrier with module
2. Open Vivado Project with "vivado_open_existing_project_guimode.cmd" or if not created, create with "vivado_create_project_guimode.cmd"
3. Type on Vivado TCL Console: TE::pr_program_flash -swapp u-boot
   Note: To program with SDK/Vivado GUI, use special FSBL (zynqmp_fsbl_flash) on setup
   optional "TE::pr_program_flash -swapp hello_te0745" possible
4. Copy image.ub and init.sh (optional on /misc/sd) on SD-Card
   - use files from (<project foler>/_binaries_<Articel Name>)/boot_linux from generated binary folder,see: Get prebuilt boot binaries(see page 14)
   - or use prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
5. Insert SD-Card

6.1.3 SD

1. Copy image.ub,Boot.bin and init.sh (optional on /misc/sd) on SD-Card.
   - use files from (<project foler>/_binaries_<Articel Name>)/boot_linux from generated binary folder,see: Get prebuilt boot binaries(see page 14)
   - or use prebuilt file location, see <design_name>/prebuilt/readme_file_location.txt
2. Set Boot Mode to SD-Boot.
   - Depends on Carrier, see carrier TRM.
3. Insert SD-Card in SD-Slot.

11 https://wiki.trenz-electronic.de/display/PD/Xilinx+Development+Tools#XilinxDevelopmentTools-XilinxSoftwareProgrammingandDebugging

6.1.4 JTAG

Not used on this Example.

6.2 Usage

1. Prepare HW like described on section Programming(see page 14)
2. Connect UART USB (most cases same as JTAG)
3. Select SD Card as Boot Mode
   Note: See TRM of the Carrier and Module.
4. Power On PCB
   Note: 1. Zynq Boot ROM loads FSBL from SD into OCM, 2. FSBL loads U-boot from SD into DDR and program PL part, 3. U-boot load Linux from SD into DDR

6.2.1 Linux

1. Open Serial Console (e.g. putty)
   a. Speed: 115200
   b. COM Port: Win OS, see device manager, Linux OS see dmesg |grep tty (UART is *USB1)
2. Linux Console:
   Note: Wait until Linux boot finished For Linux Login use:
   a. User Name: root
   b. Password: root
3. You can use Linux shell now.
   a. I2C 0 Bus type: i2cdetect -y -r 0
   b. RTC check: dmesg | grep rtc
   c. ETH0 works with udhcpc
   d. USB type "lsusb" or connect USB2.0 device
   e. (optional) init.sh scripts: Scripts will enable SFP interface after linux booting, if file is copied on SD

6.2.2 Vivado HW Manager

- ### 6.2.3 Monitoring:

  - SI5338 CLKs:
    - Open Vivado HW-Manager and add VIO signal to dashboard (*.ltx located on prebuilt folder).Set radix from VIO signals to unsigned integer.
      Note: Frequency Counter is inaccurate and displayed unit is Hz, SI5338 CLK(0 and 3) are configured to 125MHz by default.

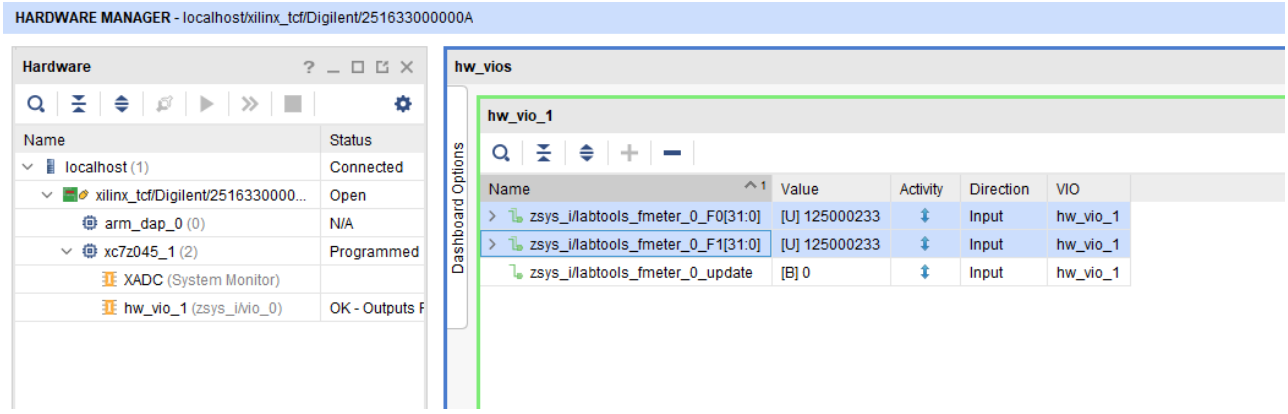


Figure 1: Vivado Hardware Manager

7 System Design - Vivado

7.1 Block Design

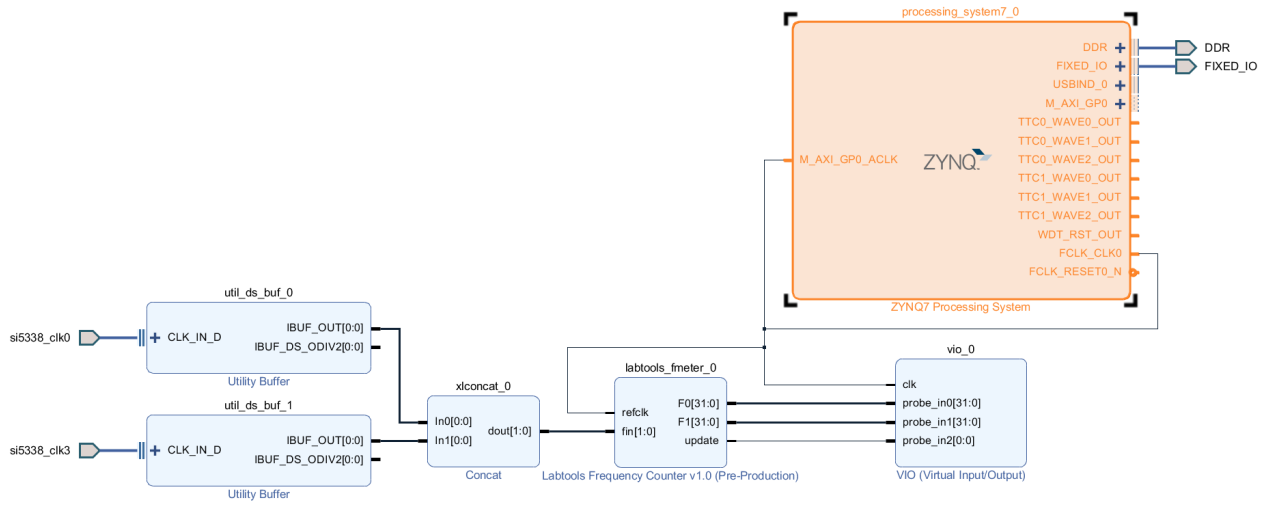


Figure 2: Block Design
*clk3 is not available on the smallest SOC (xc7z030)

7.1.1 PS Interfaces

Activated interfaces:

Type	Note
DDR	
QSPI	MIO
ETH0	MIO
USB0	MIO
SD0	MIO
UART0	MIO

Type	Note
I2C0	MIO
GPIO	MIO
ETH0 Reset	MIO
USB0 Reset	MIO
I2C0 Reset	MIO
TTC0..1	EMIO
SWDT0	EMIO

Table 10: PS Interfaces

7.2 Constrains

7.2.1 Basic module constrains

_i_bitgen_common

```
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property CONFIG_VOLTAGE 1.8 [current_design]
set_property CFGBVS GND [current_design]
```

7.2.2 Design specific constrain

_i_timing.xdc

```
set_false_path -from [get_clocks clk_fpga_0] -to [get_clocks si5338_clk0_clk_p]
set_false_path -from [get_clocks clk_fpga_0] -to [get_clocks si5338_clk3_clk_p]
set_false_path -from [get_clocks si5338_clk0_clk_p] -to [get_clocks clk_fpga_0]
set_false_path -from [get_clocks si5338_clk3_clk_p] -to [get_clocks clk_fpga_0]
```

8 Software Design - Vitis

For SDK project creation, follow instructions from:

Vitis[12]

8.1 Application

Template location: ./sw_lib/sw_apps/

8.1.1 zynq_fsbl

TE modified 2019.2 FSBL

General:

- Modified Files:main.c, fsbl_hooks.h/.c (search for 'TE Mod' on source code)
- Add Files: te_fsbl_hooks.h/.c(for hooks and board)\n\
- General Changes:
    - Display FSBL Banner and Device ID

Module Specific:

- Add Files: all TE Files start with te_*
    - Si5338 Configuration

8.1.2 zynq_fsbl_flash

TE modified 2019.2 FSBL

General:

- Modified Files: main.c
- General Changes:
    - Display FSBL Banner
    - Set FSBL Boot Mode to JTAG
    - Disable Memory initialisation

8.1.3 hello_te0745

Hello TE0745 is a Xilinx Hello World example as endless loop instead of one console output.

8.1.4 u-boot

U-Boot.elf is generated with PetaLinux. SDK/HSI is used to generate Boot.bin.

12 https://wiki.trenz-electronic.de/display/PD/Vitis

9 Software Design - PetaLinux

For PetaLinux installation and project creation, follow instructions from:

- PetaLinux KICKstart[13]

9.1 Config

Start with **petalinux-config** or **petalinux-config --get-hw-description**

Changes:

- CONFIG_SUBSYSTEM_ETHERNET_PS7_ETHERNET_0_MAC=""

9.2 U-Boot

Start with **petalinux-config -c u-boot**

Changes:

- CONFIG_ENV_IS_NOWHERE=y
- # CONFIG_ENV_IS_IN_SPI_FLASH is not set
- CONFIG_I2C_EEPROM=y
- CONFIG_ZYNQ_GEM_I2C_MAC_OFFSET=0xFA
- CONFIG_SYS_I2C_EEPROM_ADDR=0x53
- CONFIG_SYS_I2C_EEPROM_BUS=0
- CONFIG_SYS_EEPROM_SIZE=256
- CONFIG_SYS_EEPROM_PAGE_WRITE_BITS=0
- CONFIG_SYS_EEPROM_PAGE_WRITE_DELAY_MS=0
- CONFIG_SYS_I2C_EEPROM_ADDR_LEN=1
- CONFIG_SYS_I2C_EEPROM_ADDR_OVERFLOW=0

Change platform-top.h:

9.3 Device Tree

```
/include/ "system-conf.dtsi"
/ {
  chosen {
    xlnx,eeprom = &eeprom;
  };
};

/* QSPI PHY */
&qspi {
    #address-cells = <1>;
    #size-cells = <0>;
    status = "okay";
    flash0: flash@0 {
```

13 https://wiki.trenz-electronic.de/display/PD/PetaLinux+KICKstart

```
        compatible = "jedec,spi-nor";
        reg = <0x0>;
        #address-cells = <1>;
        #size-cells = <1>;
    };
};


/* ethernet */
&gem0 {
    phy-handle = <&phy0>;
    mdio {
        #address-cells = <1>;
        #size-cells = <0>;
        phy0: phy@1 {
            compatible = "marvell,88e1510";
            device_type = "ethernet-phy";
            reg = <1>;
        } ;
    } ;
};

/* usb */
/{
    usb_phy0: usb_phy@0 {
        compatible = "ulpi-phy";
        #phy-cells = <0>;
        reg = <0xe0002000 0x1000>;
        view-port = <0x0170>;
        drv-vbus;
    };
};

&usb0 {
    dr_mode = "host";
    //dr_mode = "peripheral";
    usb-phy = <&usb_phy0>;
};


/* I2C */

&i2c0 {
    #address-cells = <1>;
    #size-cells = <0>;

    rtc0: rtc@6F {
        compatible = "isl12022";
        reg = <0x6F>;
    };
      //MAC EEPROM
      eeprom: eeprom@53 {
        compatible = "atmel,24c08";
        reg = <0x53>;
      };
    i2cmux_SFP: i2cmux@72  {
```

```
        compatible = "nxp,pca9548";
        #address-cells = <1>;
        #size-cells = <0>;
        reg = <0x72>;

        SFP@0 {
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <0>;
        };
        SFP@1 {
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <1>;
        };
        SFP@2 {
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <2>;
        };
        SFP@3 {
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <3>;
        };
        SFP@4 {
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <4>;
        };
        SFP@5 {
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <5>;
        };
        SFP@6 {
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <6>;
        };
        SFP@7 {
            #address-cells = <1>;
            #size-cells = <0>;
            reg = <7>;
        };
    };

};
```

9.4 Kernel

Start with **petalinux-config -c kernel**

Changes:

- CONFIG_RTC_DRV_ISL12022=y

9.5 Rootfs

Start with **petalinux-config -c rootfs**

Changes:

- i2c-tools
- CONFIG_busybox-httpd=y (for web server app)
- CONFIG_packagegroup-petalinux-utils(util-linux,cpufrequtils,bridge-utils,mtd-utils,usbutils,pciutils,canutils,i2c-tools,smartmontools,e2fsprogs)

9.6 Applications

9.6.1 startup

Script App to load init.sh from SD Card if available.

9.6.2 webfwu

Webserver application accemble for Zynq access. Need busybox-httpd

10 Additional Software

10.1 SI5338

File location <design name>/misc/Si5338/Si5338-*.slabtimeproj

General documentation how you work with these project will be available on Si5338[14]

14 https://wiki.trenz-electronic.de/display/PD/Si5338

11 Appx. A: Change History and Legal Notices

11.1 Document Change History

To get content of older revision got to "Change History" of this page and select older document revision number.

Date	Document Revision	Authors	Description
2020-03-30	v.13 (see page 6)	John Hartfiel[15]	• Release 2019.2
2019-09-18	v.12	John Hartfiel	• bugfix for TE0745-02-45-3EA
2018-12-19	v.11	John Hartfiel	• documentation notes
2018-11-26	v.10	John Hartfiel	• update 2018.2 • documentation style update
2018-04-09	v.7	John Hartfiel	• Typo correction
2018-02-09	v.6	John Hartfiel	• Release 2017.2
2017-09-11	v.1	John Hartfiel	• Initial release
--	all	John Hartfiel[16]	--

Table 11: Document change history.

11.2 Legal Notices

11.3 Data Privacy

Please also note our data protection declaration at https://www.trenz-electronic.de/en/Data-protection-Privacy

15 https://wiki.trenz-electronic.de/display/~j.hartfiel
16 https://wiki.trenz-electronic.de/display/~j.hartfiel

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17 http://guidance.echa.europa.eu/

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WEEE

Information for users within the European Union in accordance with Directive 2002/96/EC of the European Parliament and of the Council of 27 January 2003 on waste electrical and electronic equipment (WEEE).

Users of electrical and electronic equipment in private households are required not to dispose of waste electrical and electronic equipment as unsorted municipal waste and to collect such waste electrical and electronic equipment separately. By the 13 August 2005, Member States shall have ensured that systems are set up allowing final holders and distributors to return waste electrical and electronic equipment at least free of charge. Member States shall ensure the availability and accessibility of the necessary collection facilities. Separate collection is the precondition to ensure specific treatment and recycling of waste electrical and electronic equipment and is necessary to achieve the chosen level of protection of human health and the environment in the European Union. Consumers have to actively contribute to the success of such collection and the return of waste electrical and electronic equipment. Presence of hazardous substances in electrical and electronic equipment results in potential effects on the environment and human health. The symbol consisting of the crossed-out wheeled bin indicates separate collection for waste electrical and electronic equipment.

Trenz Electronic is registered under WEEE-Reg.-Nr. DE97922676.

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